EE 505

Lecture 20

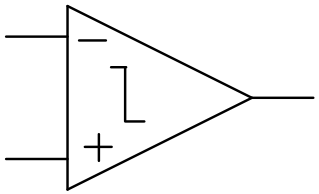
ADC Design

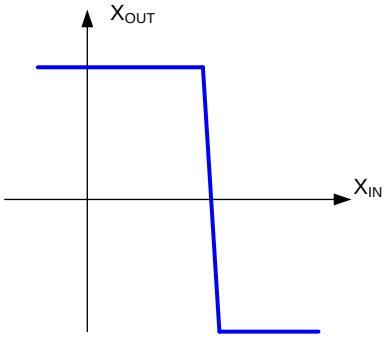
- The Flash ADC

Review from Last Lecture

Analog to Digital Converters

The conversion from analog to digital in ALL ADCs is done with comparators

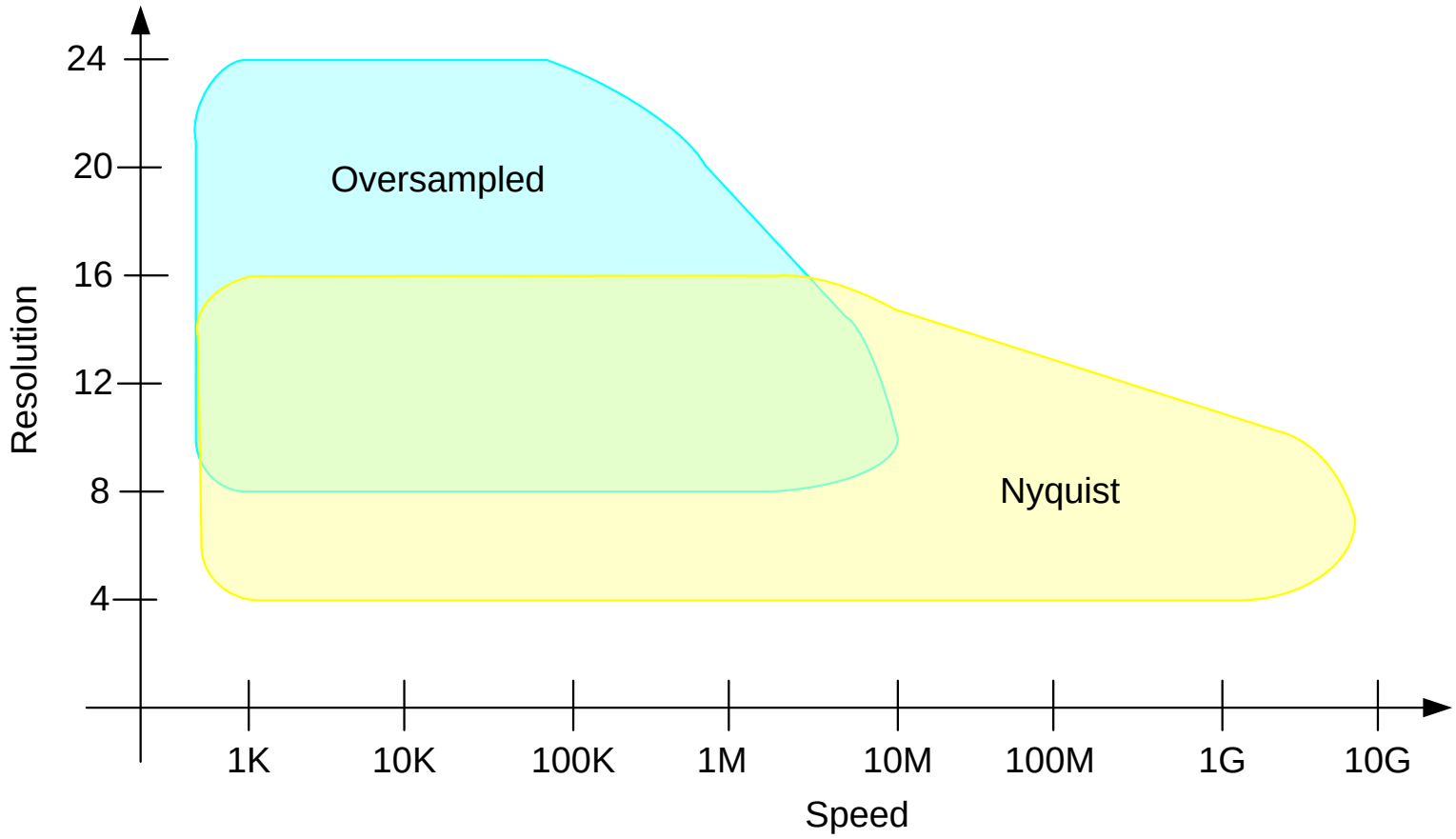




ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

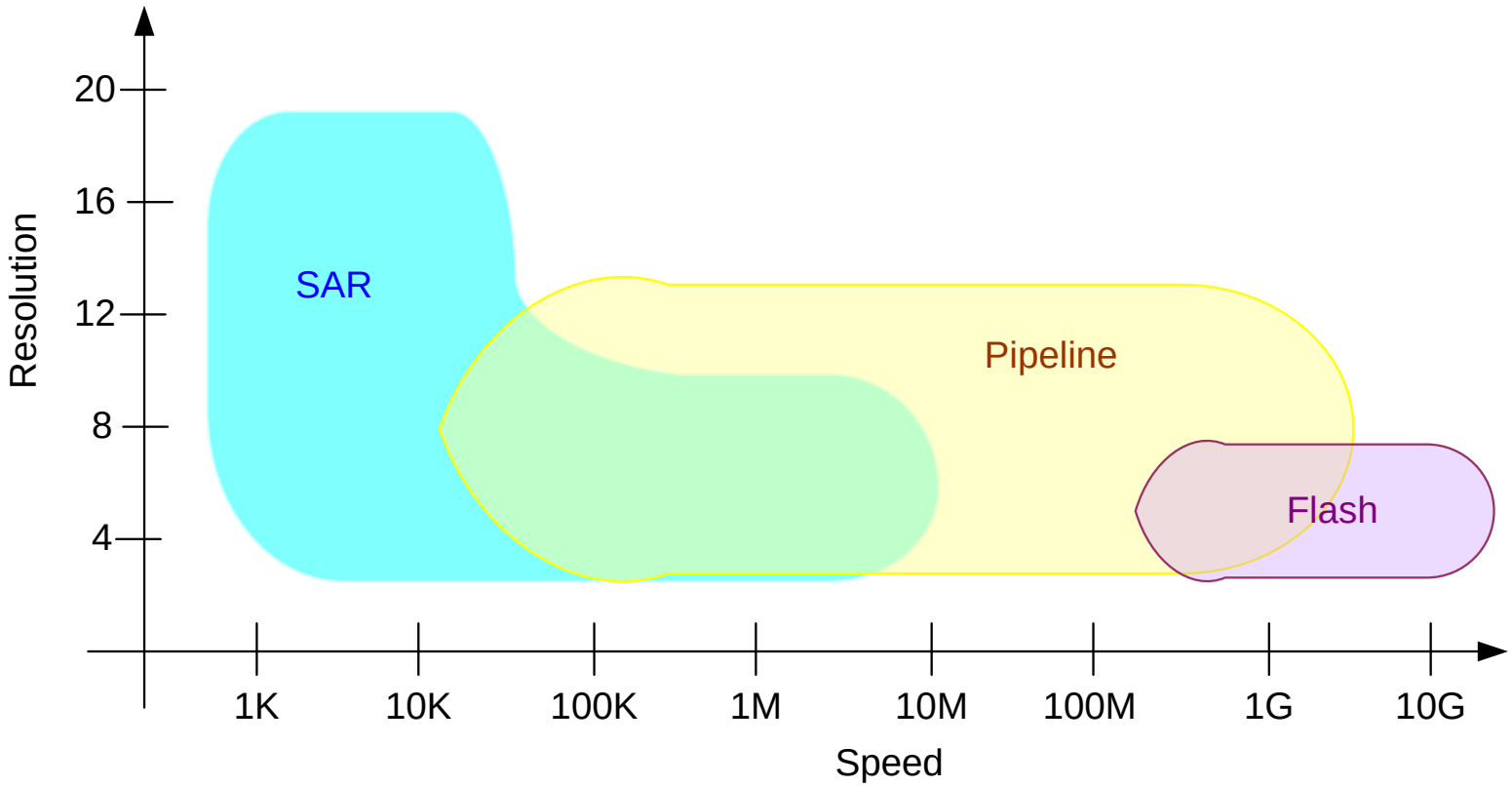
Review from Last Lecture

Data Converter Type Chart



Review from Last Lecture

Nyqyist Rate Usage Structures



Flash is the least used as a stand-alone structure but widely used as a subcomponent in SAR and Pipelined Structures

Review from Last Lecture

ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

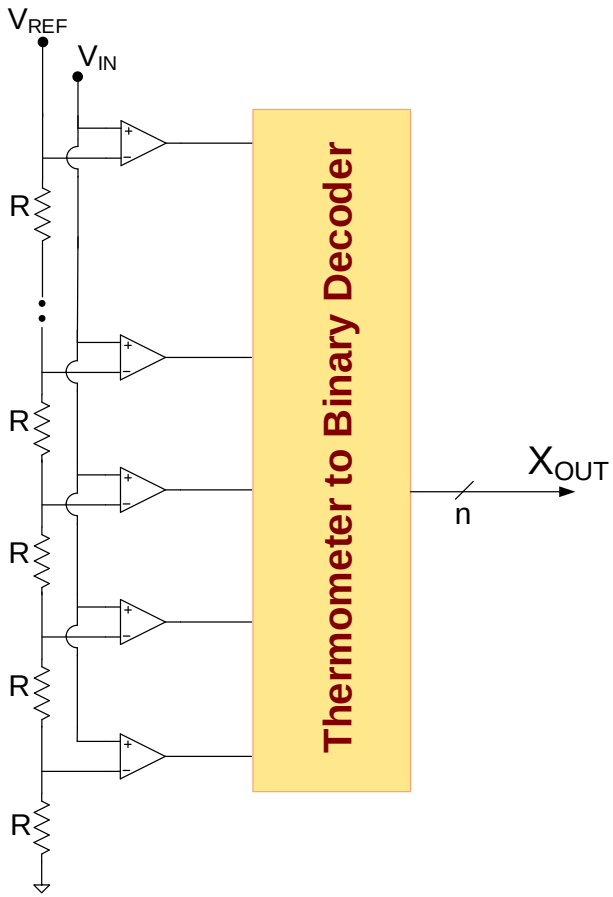
- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

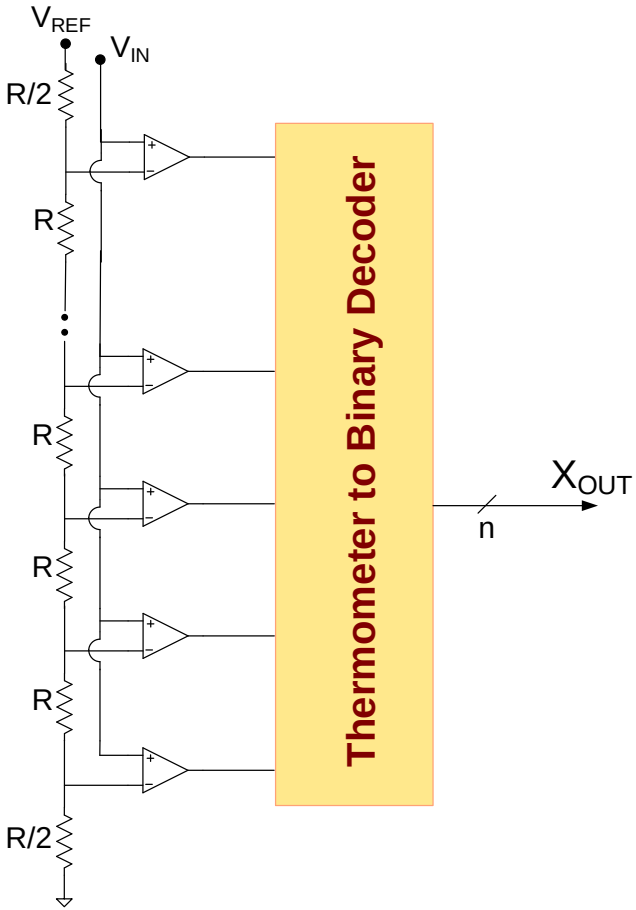
All have comparable conversion rates

Basic approach in all is very similar

Review from Last Lecture

Flash ADC

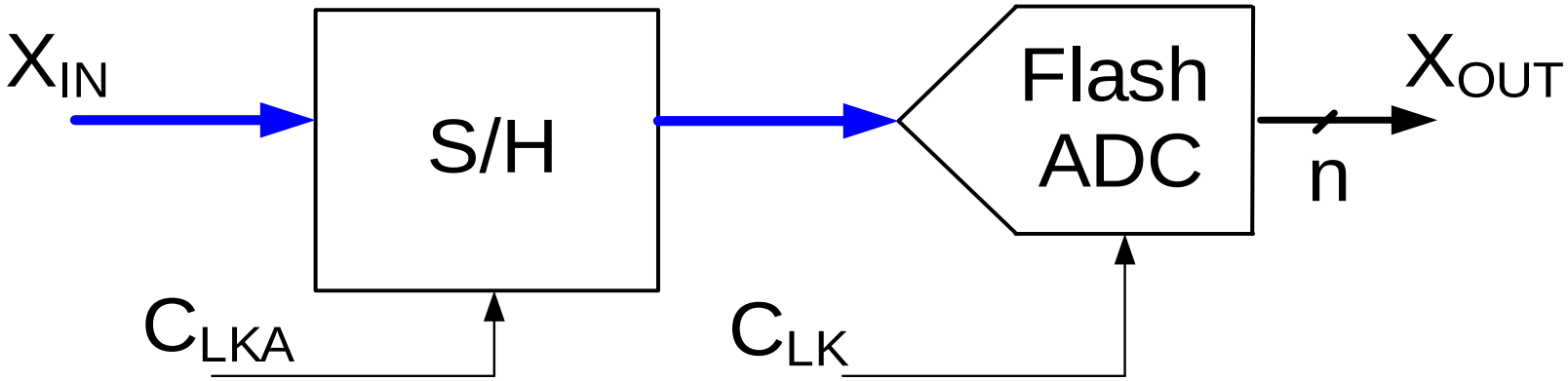




Review from Last Lecture

Input change during conversion

Front-End S/H can mitigate effects of input change during conversion

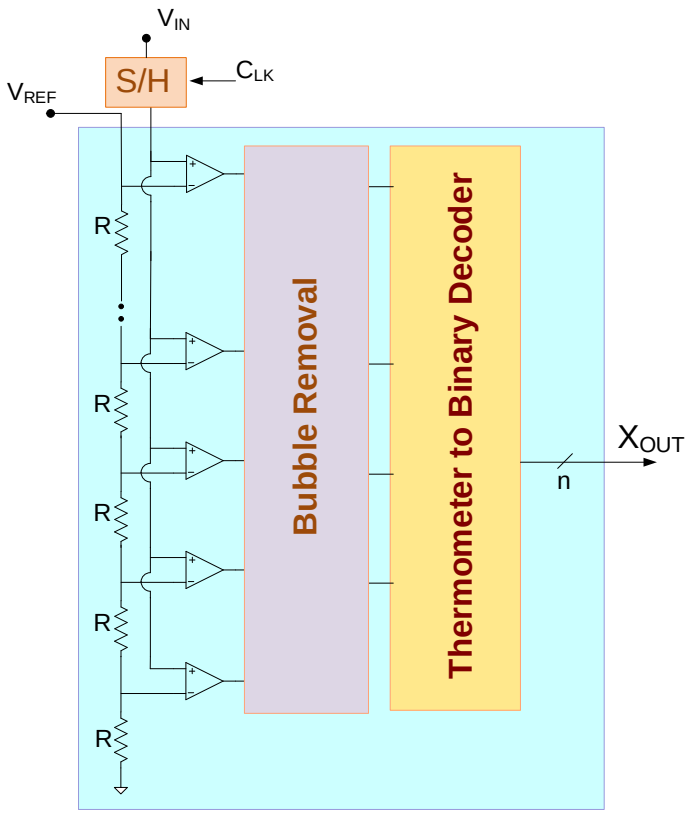


- Speed of sample/hold of concern
- Noise of S/H
- Nonlinearity of S/H
- Input range of S/H
- Power dissipation of S/H
- Loose asynchronous operation of ADC
- Widely used
- S/H may be most challenging part of design

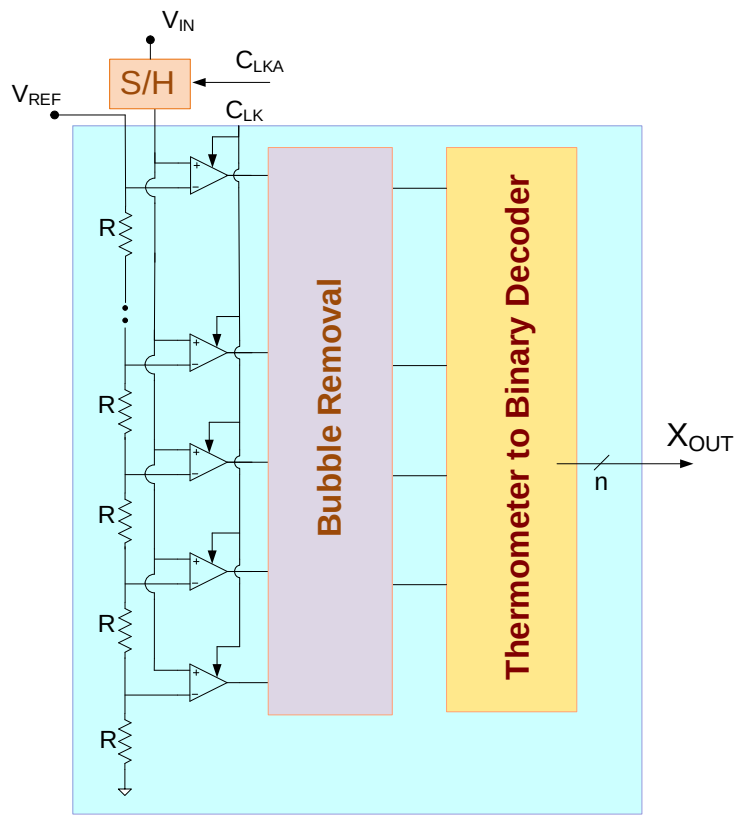
Review from Last Lecture

Input change during conversion

Flash ADC with Front-End S/H

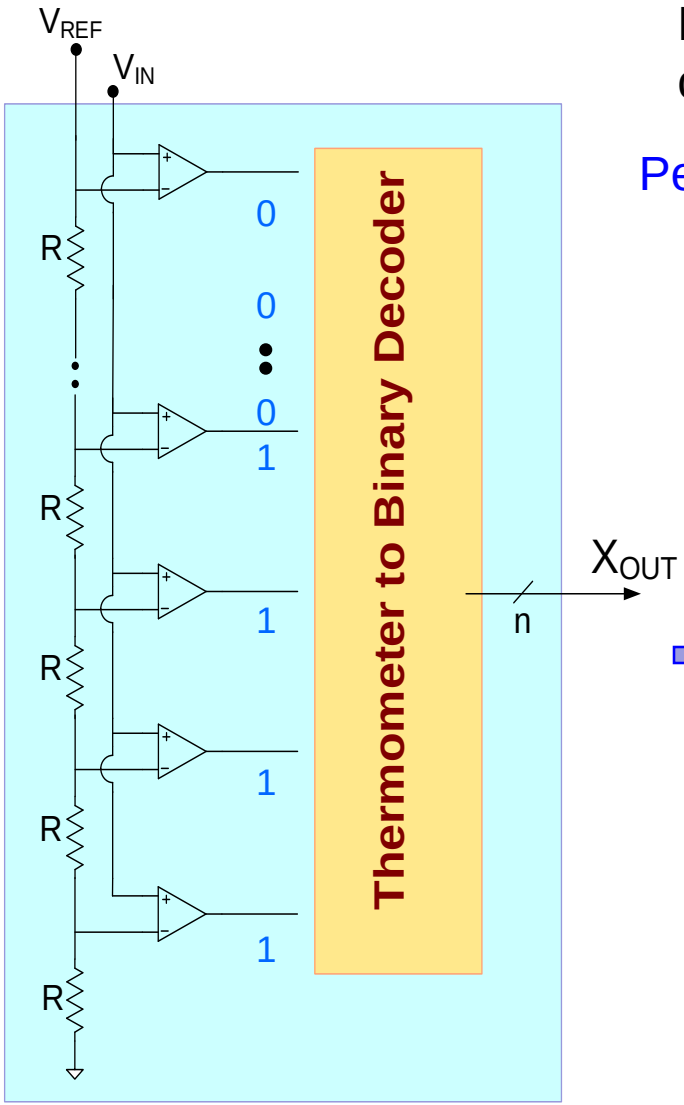


Input S/H with Clk



Input S/H with Clk and clocked comparators

Flash ADC



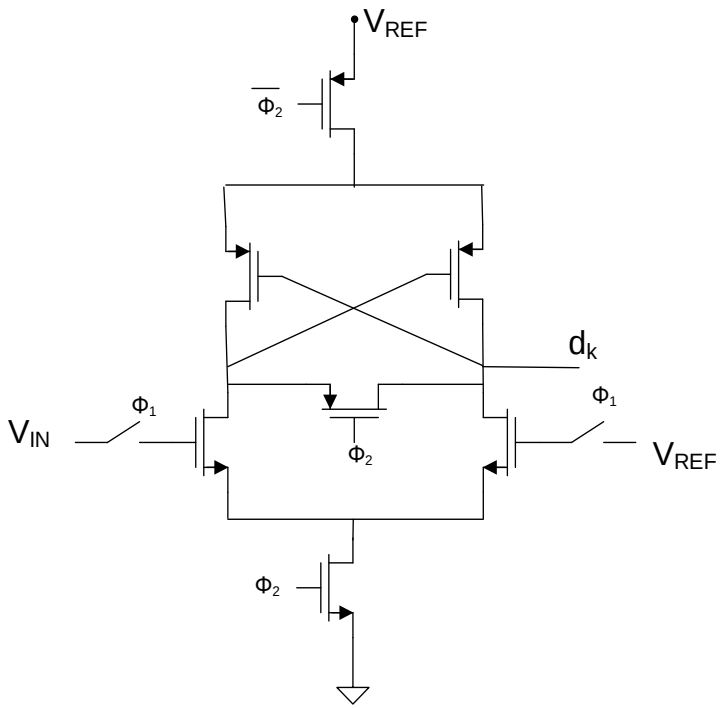
Basic structure has thermometer code at output

Performance Issues:

+ Very fast
+ Simple architecture
+ Instantaneous (asynchronous output)
+ Good DNL with low comparator offsets

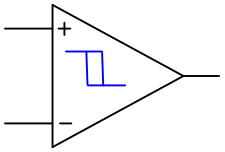
− Bubble vulnerability
− Input change during conversion
− Wide range of common-mode comparator inputs
− Number of components and area (for large n)
− Loading of V_{REF} and V_{IN}
− Propagation of V_{IN}
− Power dissipation (for large n)
− Offset and speed of comparators
− Layout of resistors
− Voltage and temperature dependence of R's
− Matching of R's

Clocked Comparator with Regenerative Feedback

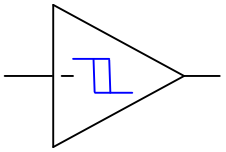


Regenerative Feedback

Regenerative Comparators



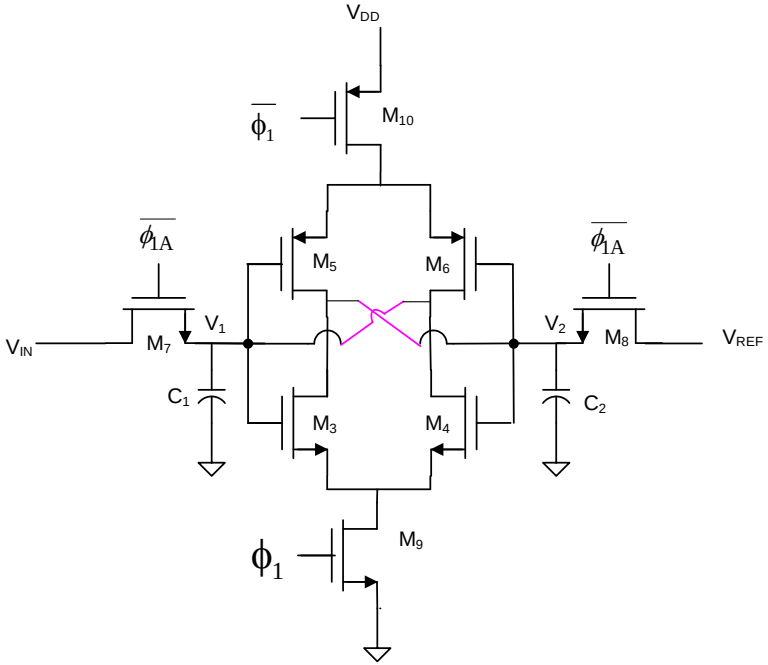
Differential

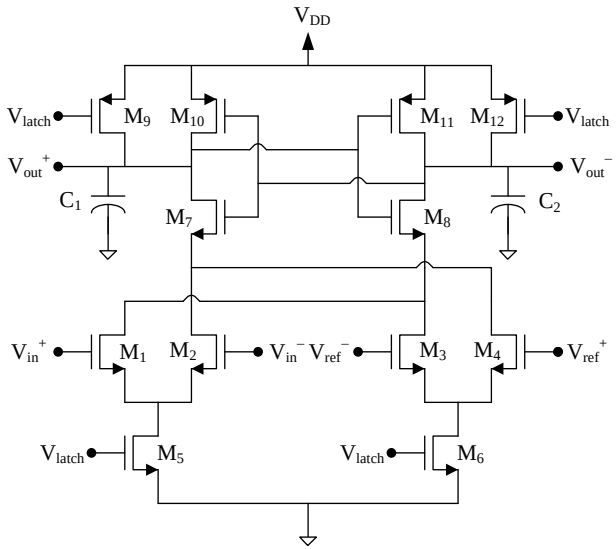


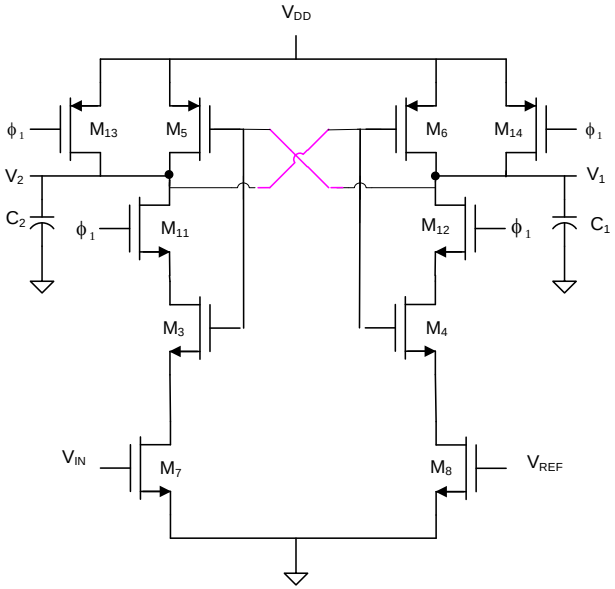
Single-Ended

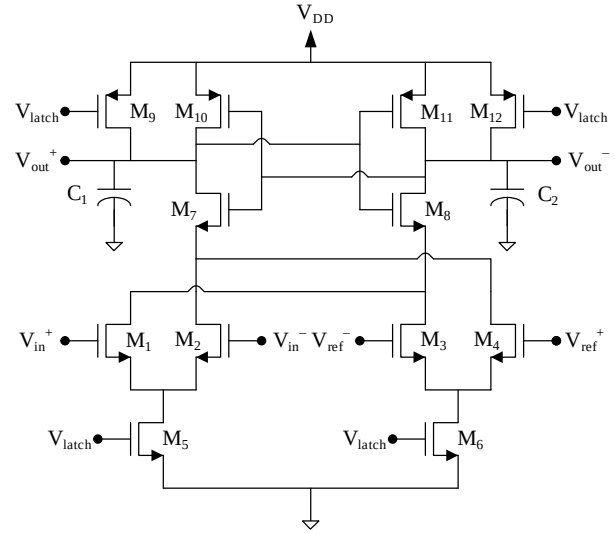
- Regenerative feedback often used to force decision when differential inputs are small
- Several variants of clocked comparators are available
- Important to not have trip point dependent upon previous comparison results
- Often one or more linear gain stages precede the regenerative stage
- Power dissipation can be small in regenerative feedback comparators
- Large offset voltage (100mV or more) common for regenerative feedback comparators

Clocked Comparator with Regenerative Feedback

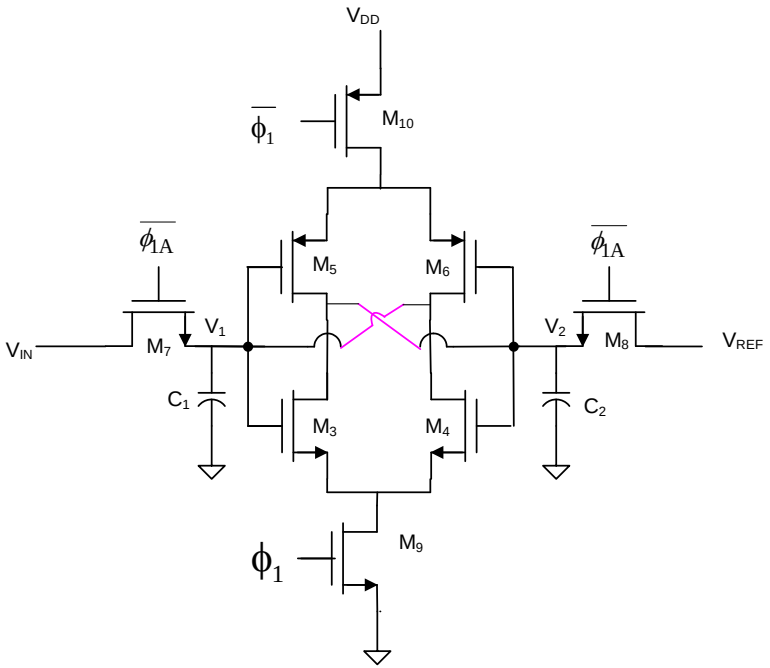






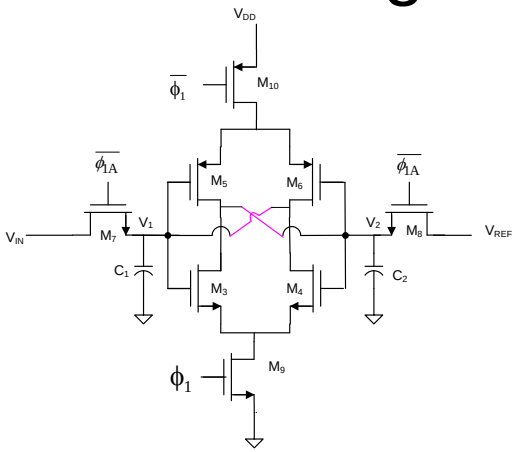


Clocked Comparator with Regenerative Feedback

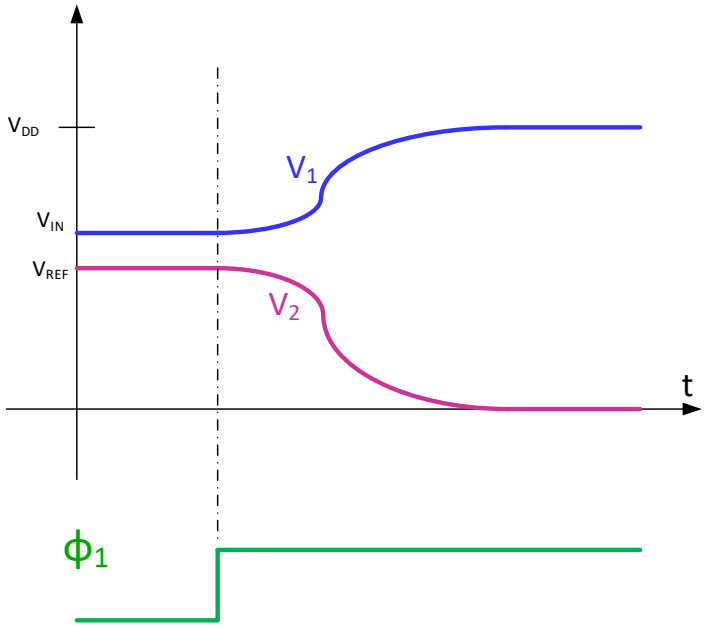


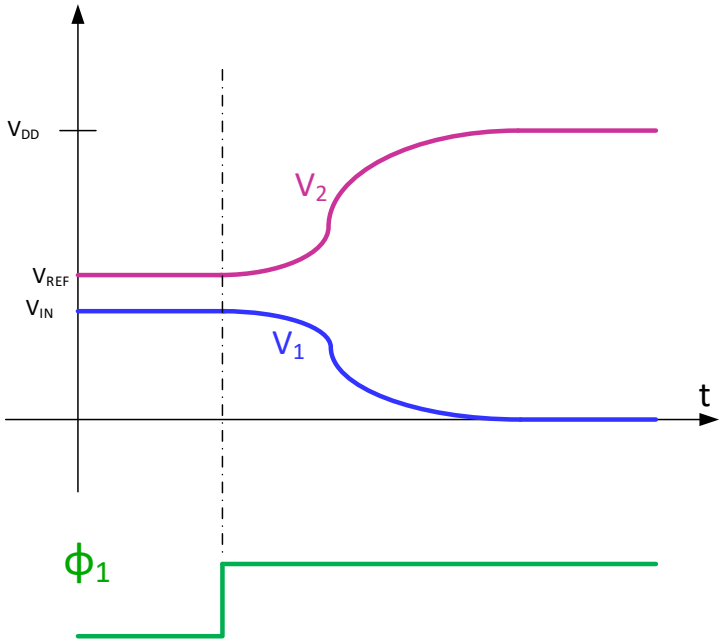
Advanced clock samples inputs on input to digital latch cell
During regenerative state power dissipation goes to 0 after decision is made

Clocked Comparator with Regenerative Feedback

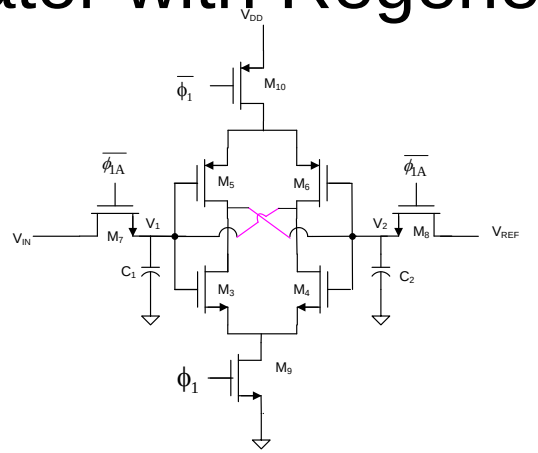


Desired Response

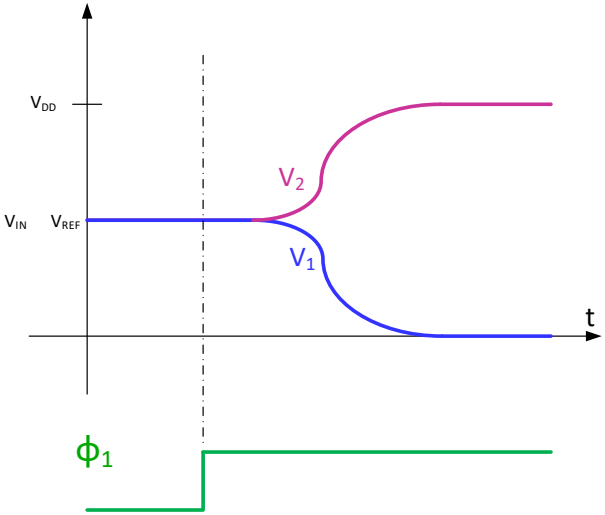


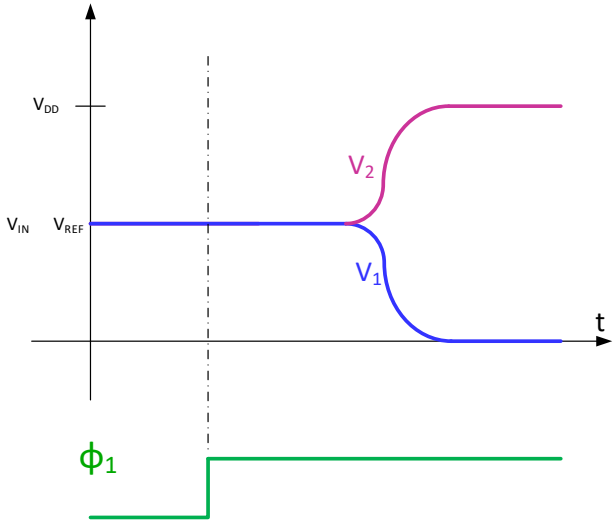


Clocked Comparator with Regenerative Feedback



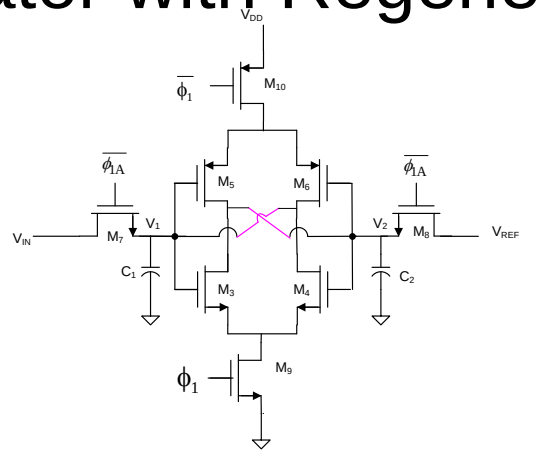
when V_{IN} and V_{REF} close to each other



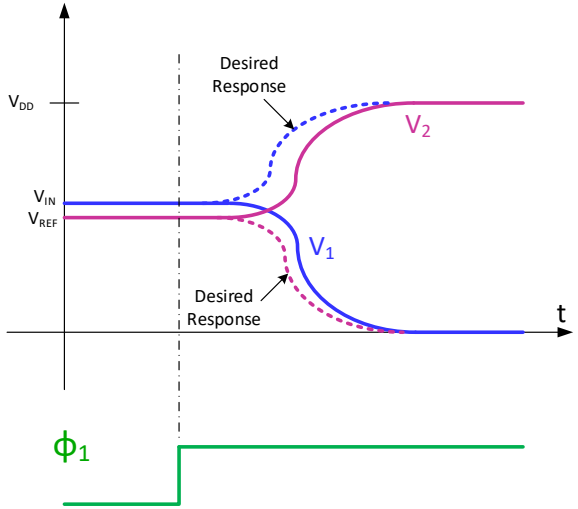


- decision delayed
- may stay in metastable state until after decision must be made
- vulnerable to making wrong decision due to offset or noise

Clocked Comparator with Regenerative Feedback

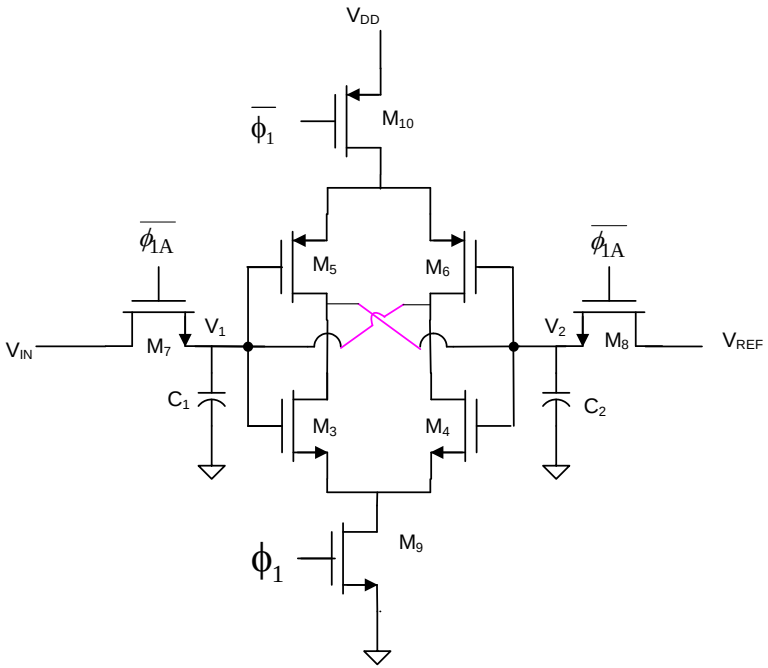


when V_{IN} and V_{REF} close to each other



- wrong decision when close (exaggerated)
- almost always only concerned about when V_{IN} close to V_{REF}

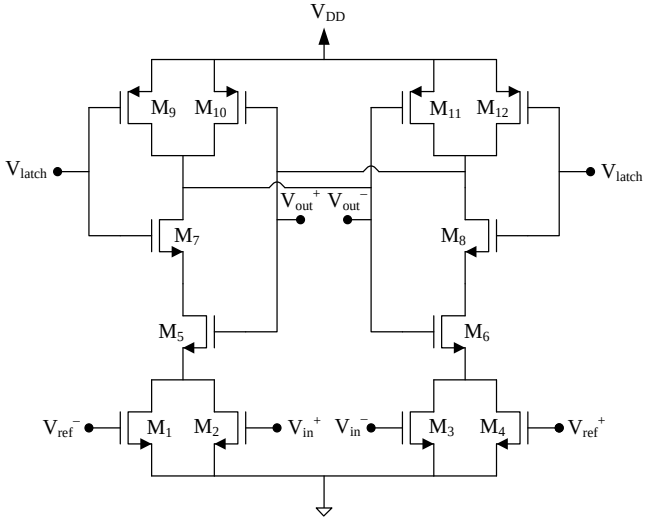
Clocked Comparator with Regenerative Feedback



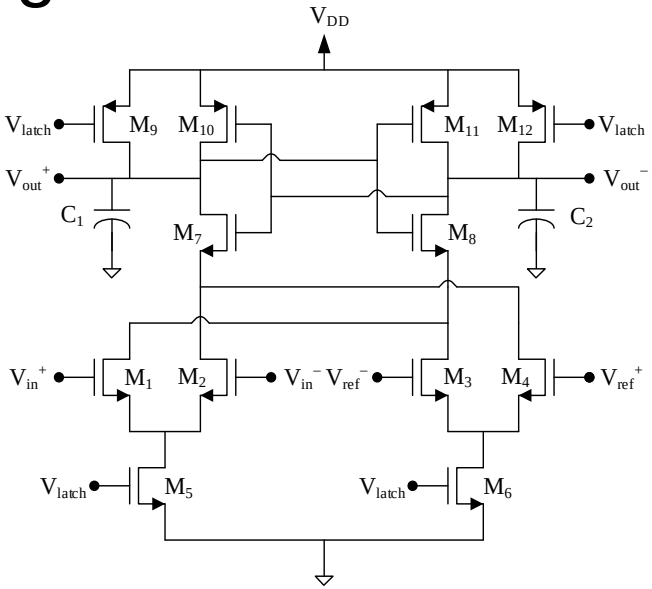
Dominant causes of offset voltage of comparator

- Missmatch of parasitic capacitance on V_1 and V_2 nodes
- Missmatch in digital inverter trip points (particularly in weak inversion)
- Missmatch on advanced clocks (timing and parasitic capacitances)
- Missmatch of charge injection of advanced clocks
- Missmatch of leakage diffusion currents
- Assymetry in layout of cross-coupled structures
- Noise when in weak inversion

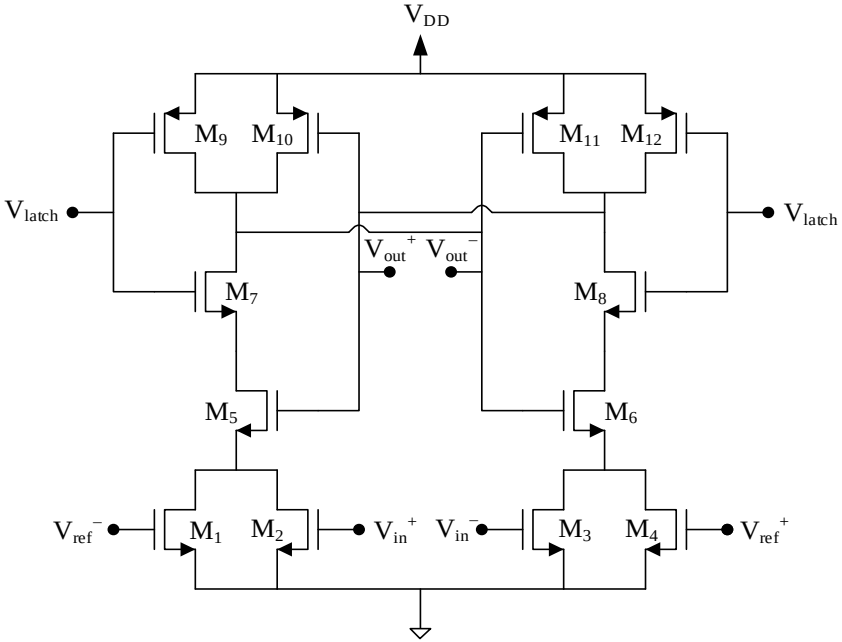
Clocked Comparator with Regenerative Feedback



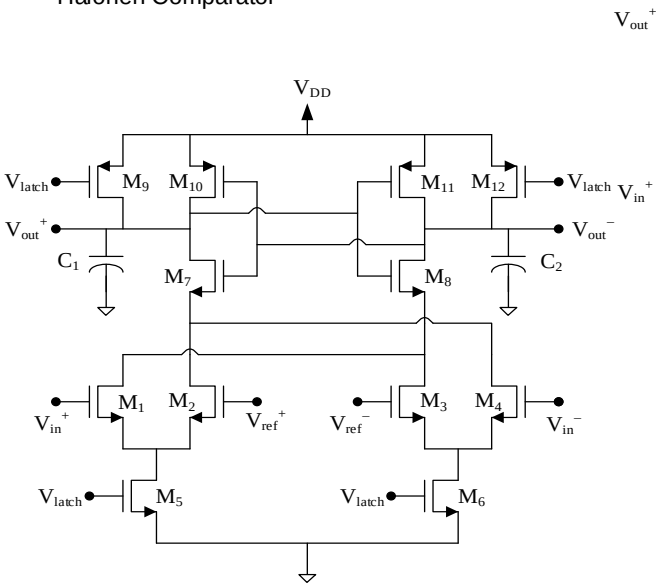
Lewis Gray Comparator



Halonen Comparator

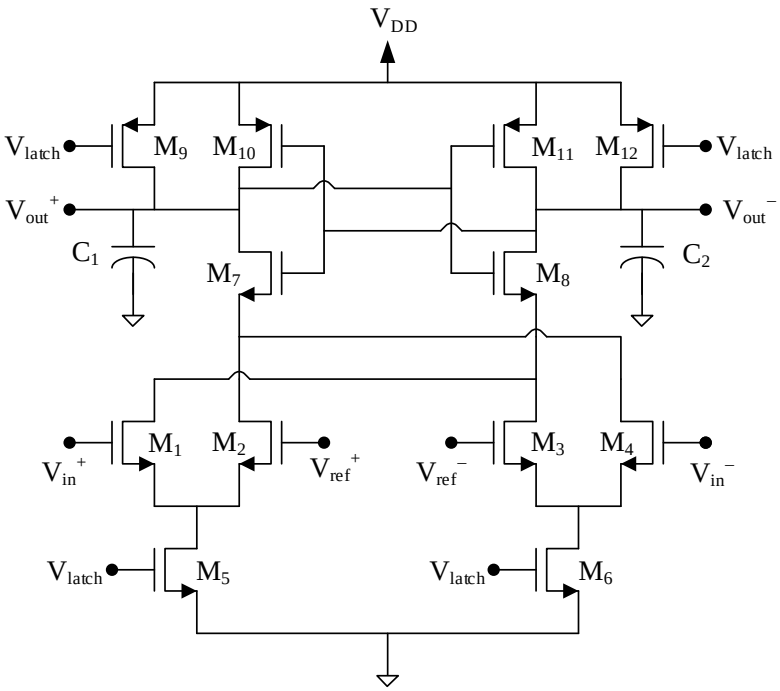


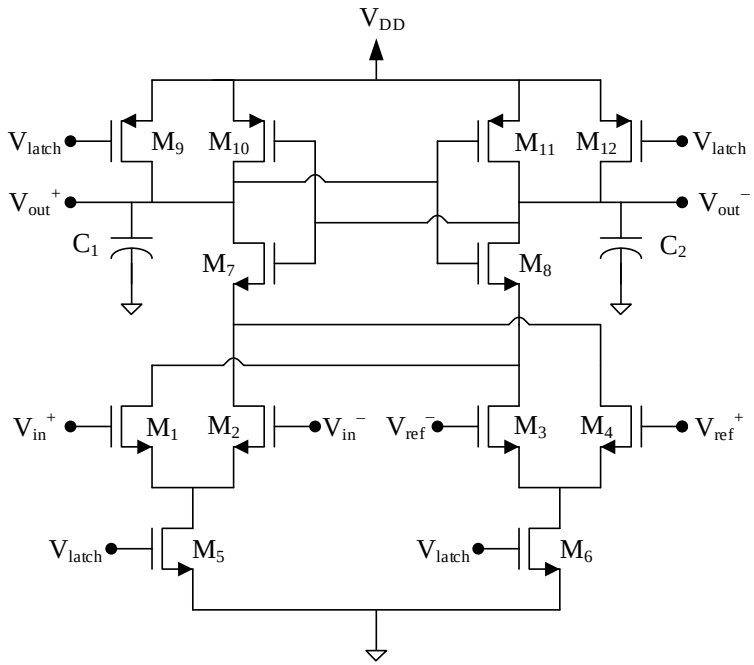
Sansen 92



Katyal Comparator

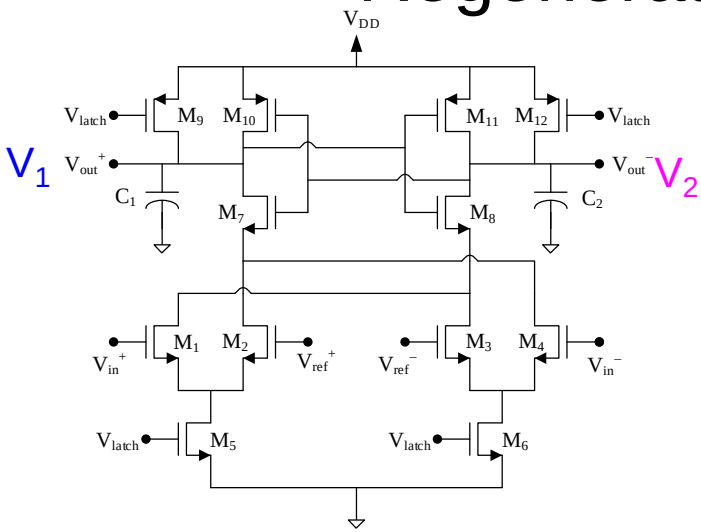
Katyal and Halonen Comparators with Regenerative Feedback

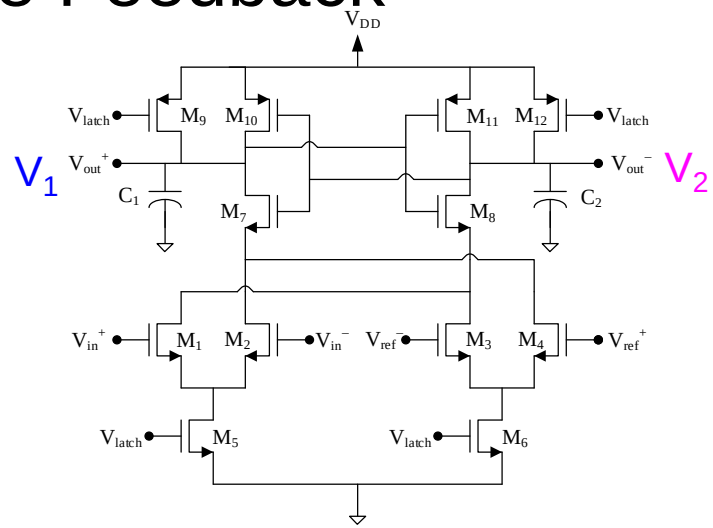




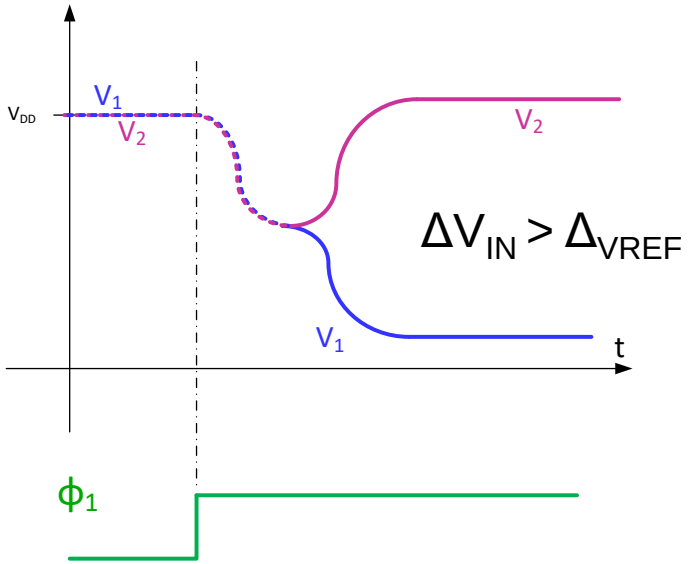
- Outputs precharge to V_{DD}
- Current is steered to left or right side depending upon input differences
- Phasing of upper latch and lower latch signal may be different
- May limit swing on latch signals (switch versus current source in tail)
- Small previous-code dependence due to residual voltages on sources of M_7 and M_8

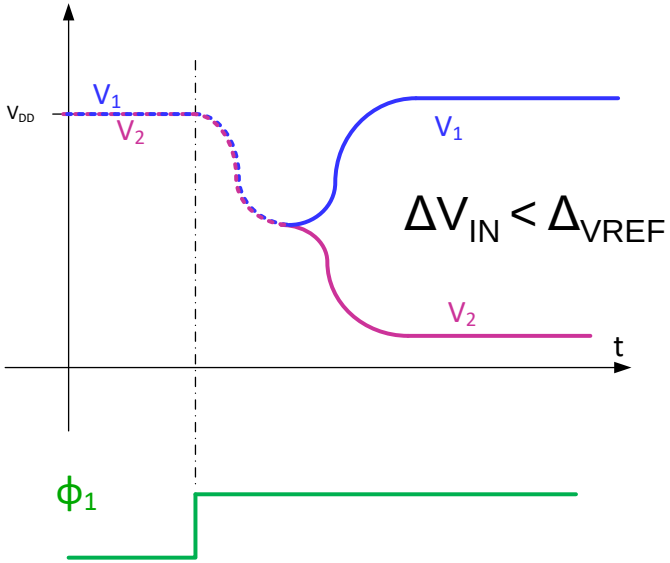
Katyal and Halonen Comparators with Regenerative Feedback



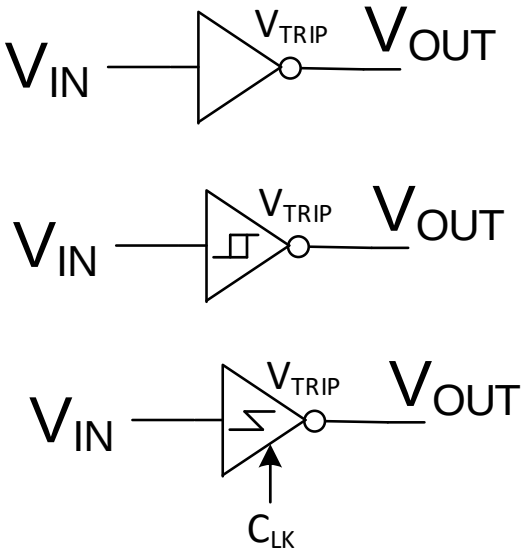


Ideal Responses



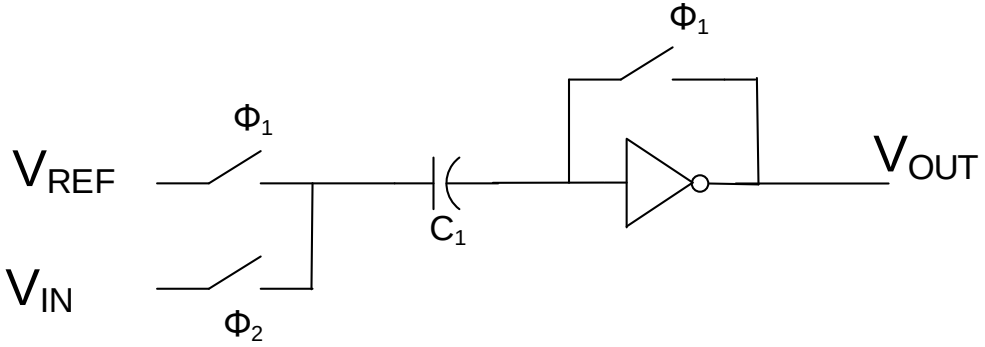


Single-Ended Comparator w/o Reference



- Reference embedded in inverter trip point
- Device dimensions can set trip point
- Could be extremely small
- Highly dependent upon process variations
- Calibration can be used to trim trip points

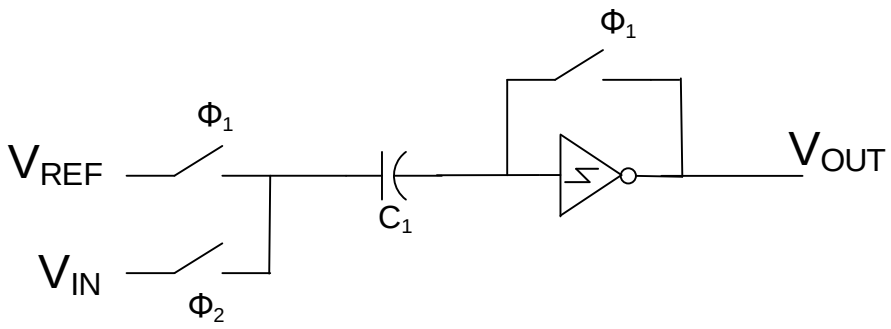
Clocked Linear Comparator with Offset Compensation



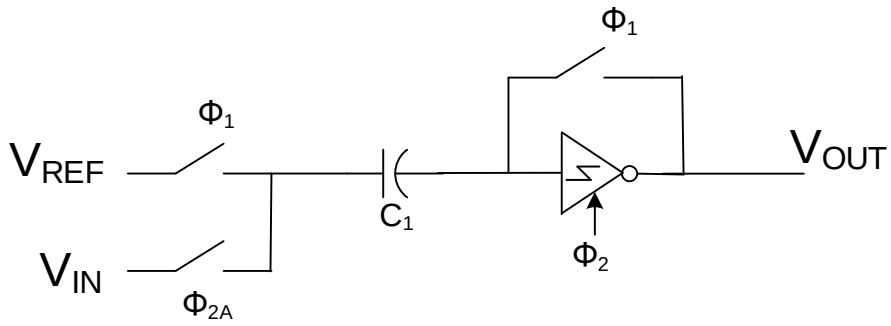
Preamplifier or Linear Comparator with offset compensation

- Ideally removes all offset effects
- May not have a large enough gain
- Offset Compensation can be added to regenerative latches
- Several variants of offset compensation circuits are available

Offset Compensation

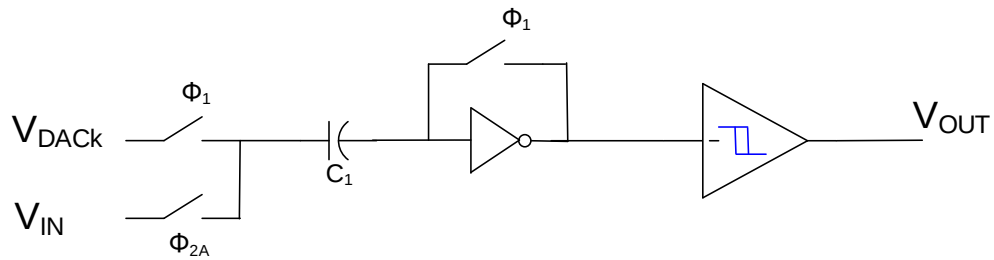


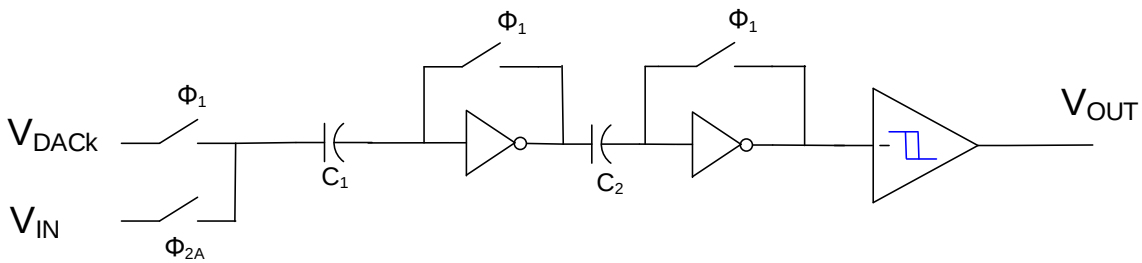
Preamplifier or Regenerative Feedback can be added to amplifier

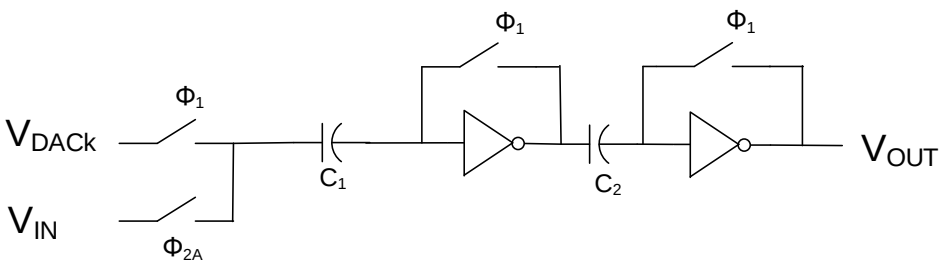


Comparator can be clocked following linear amplifier phase

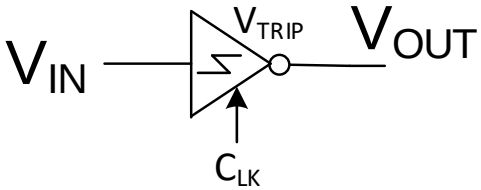
Some Variants of Clocked Offset Compensation

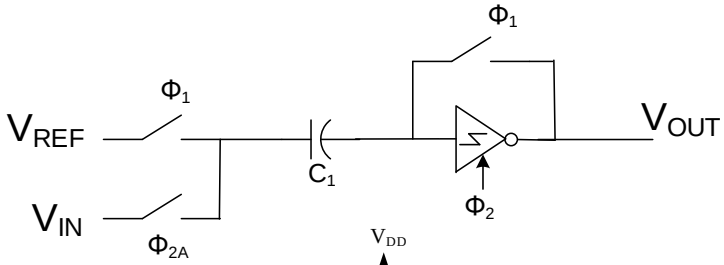


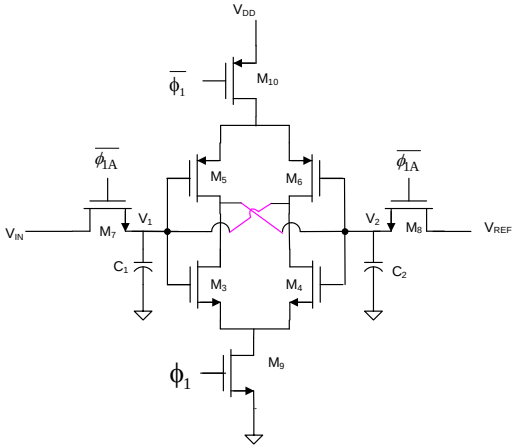


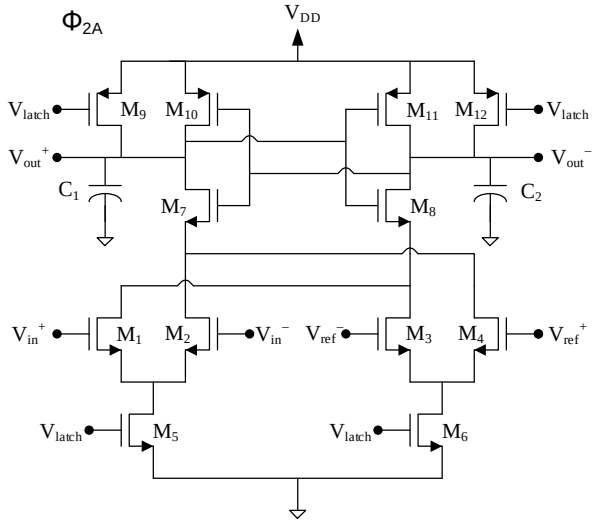


Where are poles of regenerative comparators located?









In RHP !

Is stability of concern?

No ! Want positive real axis poles (i.e. unstable circuit) to force decision

Stay Safe and Stay Healthy !

End of Lecture 20